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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/580,625	HUETING ET AL.	
	Examiner	Art Unit	
	Hsin-Yi (Steven) Hsieh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claims 15-18 and 21** are objected to because of the following informalities:

2. Claim 15 recites the limitation 'the part of a drift region" in the 4th and 5th last lines of the claim, which seems to be a typo of 'a part of the drift region".

3. Claim 21 recites the limitation 'ration" in the second line of the claim, which seems to be a typo of "ratio".

4. Claims 16-18 are objected because they depend on the objected claim 15.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. **Claim 21** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 21 recites "the drift region has a steeply graded doping concentration that is defined by the ration of the doping concentration of the part of the drift region adjacent to the body region to the doping concentration of the part of the drift region adjacent to the drain region and wherein the

ratio is greater than at least one of: 50, 100 or 200," which lacks the full support of the original disclosure. The specification indicates that the doping concentration in the drift region is such that the doping concentration adjacent to the drift region is higher than the doping concentration adjacent to the body region by a factor of at least 50 [page 3 lines 6-10], at least 100 [page 3 lines 14-19], at least 200 [page 3 lines 14-19], 100 [page 9 lines 12-18; page 10 lines 1-6], or 200 [page 7 lines 21-26], which means the ratio of the doping concentration of the part of the drift region adjacent to the body region to the doping concentration of the part of the drift region adjacent to the drain region should be less than at least one of: 1/50, 1/100, or 1/200.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 5-6, 10 and 21** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 5 recites the limitation "the surface" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 10 recites the limitation "the cell pitch" in the first two lines of the claim. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 21 recites "the drift region has a steeply graded doping concentration that is defined by the ration of the doping concentration of the part of the drift region adjacent to the body region to the doping concentration of the part of the drift region adjacent to the drain region and wherein the ratio is greater than at least one of: 50, 100 or 200," which is inconsistent with the specification. The specification indicates that the doping concentration in the drift region is

such that the doping concentration adjacent to the drift region is higher than the doping concentration adjacent to the body region by a factor of at least 50 [page 3 lines 6-10], at least 100 [page 3 lines 14-19], at least 200 [page 3 lines 14-19], 100 [page 9 lines 12-18; page 10 lines 1-6], or 200 [page 7 lines 21-26], which means the ratio of the doping concentration of the part of the drift region adjacent to the body region to the doping concentration of the part of the drift region adjacent to the drain region is less than at least one of: 1/50, 1/100, or 1/200. This inconsistency renders the claim indefinite.

12. Claim 6 is rejected because it depends on the rejected claim 5.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. **Claims 1, 4-7, 9-10, 12-19 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. (EP 1168455 A2) as can be understood since claims 5-6, 10 and 21 have been rejected under 35 U.S.C. 112.

16. Regarding **claim 1**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of a first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of a second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of the first conductivity type (n-type; paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of the first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11) past the source region (14) and the body region (13) into the drift region (12), each insulated trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18;

Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode (19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and a doping concentration in the drift region (12) increases from a part of the drift region (12) adjacent to the body region (13) to a part of the drift region (12) adjacent to the drain region (11; see Fig. 15B, paragraph [0053]),

Omura et al. do not teach the gate-field plate insulator (18) being at least as thick as the field plate insulator (16), and the doping concentration in the drift region (12) being at least 50 times greater adjacent to the drain region (11) than adjacent to the body region (13).

Parameters such as the thicknesses of the gate-field plate insulator and the filed plate insulator, and the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the breakdown voltage and the threshold voltage in paragraph [0031]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thicknesses of the gate-field plate insulator and the filed plate insulator and the doping concentration within the range as claimed in order to achieve desired device performance.

17. Regarding **claim 4**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein a breakdown voltage of the insulated gate field effect transistor is less than or equal to 30V.

Omura et al. teach a device with a breakdown voltage of 50V (paragraph [0045]). Omura et al. also teach that the breakdown voltage and the ON resistance satisfy the inequality: Ron < 2.2×10^{-5} $Vb^{2.25}$.

Parameters such as the breakdown voltage and the ON resistance in the art of semiconductor manufacturing process are the tradeoff between the device's performance and reliability and are subject to changes due to the requirement of the application, e.g. whether the performance (lower ON resistance) is more important than the reliability (higher break down voltage). Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to lower the breakdown voltage to less than or equal to 30V as claimed in order to achieve a lower ON resistance to improve device performance.

18. Regarding **claim 5**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the pattern of cells defined by the source regions (14) and the insulated trenches (15) arranged across the first major surface (the top surface of 13) is a pattern in which cells repeat in more than one direction across the surface to form a three-dimensional cell structure (see Fig. 25).

19. Regarding **claim 6**, Omura et al. also teach an insulated gate field effect transistor according to claim 5 wherein the cells are arranged in a hexagonal pattern (see Fig. 25)

20. Regarding **claim 7**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising an additional trench (the trench formed between the

interlevel dielectric films 22; Fig. 4; paragraph [0026]) filled with conductive material (the conductive material of the source electrode 21; Fig. 4, paragraph [0026]) extending through the source region (14) to the body region (13) to connect a source contact (source electrode 21) to the source region (14) and the body region (13; see Fig. 4).

21. Regarding **claim 9**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein a thickness of the insulator (16; Fig. 2) adjacent to the conductive field plate electrode (17) is greater than a thickness of the insulator (18) adjacent to the conductive gate electrode (19; see Fig. 2, paragraph [0031]).

22. Regarding **claim 10**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the cell pitch is not greater than 1 micron.

Parameters such as the cell pitch in the art of semiconductor manufacturing process are subject to change due to the requirement of the device performance. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to use a cell pitch not greater than 1 micron as claimed to achieve the required performance.

23. Regarding **claim 12**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the field plate insulator (16) has a thickness between 0.6 to 1 microns and the gate insulator (18) has a thickness between 0.2 to 0.5 microns.

Omura et al. teach that the thickness of the field plate oxide (16) is determined by the breakdown voltage and the thickness of the gate oxide (18) is determined by the threshold voltage (paragraph [0031]) Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to have the thickness of the field plate oxide and the

thickness of the gate oxide as claimed as a result of achieving a desired or required breakdown voltage and threshold voltage.

24. Regarding **claim 13**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the conductive field plate electrode (17) is connected to the source region (21; Fig. 3, paragraph [0026])

25. Regarding **claim 14**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising a field plate terminal connected to the conductive field plate electrode for controlling a field plate voltage independently (this is implied in the paragraph [0027], where Omura et al. disclose a voltage applied to each buried electrode 17, which obviously need a terminal connected to the buried electrode 17 to control the voltage).

26. Regarding **claim 15**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of a first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of a second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of the first conductivity type (n-type; paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of the first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom

surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11) past the source region (14) and the body region (13) into the drift region (12), each insulated trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode(19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and wherein the drift region (12) has a graded doping concentration (see Fig. 15B) that increases from the part of a drift region (12) adjacent to the body region (13) to a part of the drift region (12) adjacent to the drain region (11; see Fig. 15B).

Omura et al. do not teach the gate-field plate insulator (18) being thicker than the field plate insulator (16), the doping concentration in the part of the drift region (12) adjacent to the drain region (11) being at least 50 times greater than the doping concentration in the part of the drift region (12) adjacent to the body region (13).

Parameters such as the thicknesses of the gate-field plate insulator and the filed plate insulator, and the doping concentration in the art of semiconductor manufacturing process are

subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the breakdown voltage and the threshold voltage in paragraph [0031]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thicknesses of the gate-field plate insulator and the filed plate insulator and the doping concentration within the range as claimed in order to achieve desired device performance.

27. Regarding **claims 16-17**, Omura et al. teach the doping concentration (Fig. 15B), the drift region (12), the drain region (11), the body region (13).

Omura et al. do not teach, regarding to **claim 16**, wherein the doping concentration in the part of the drift region adjacent to the drain region is at least 200 times greater than the doping concentration in the part of the drift region adjacent to the body region, regarding to **claim 17**, the doping concentration in the part of the drift region adjacent to the drain region is at least 100 times greater than the doping concentration in the part of the drift region adjacent to the body region,

Parameters such as the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003], or the breakdown voltage and the threshold voltage in paragraph [0031]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the doping concentration within the range as claimed in order to achieve desired device performance.

28. Regarding **claim 18**, Omura et al. teach further comprising a source contact (source electrode 21; Fig. 4, paragraph [0026]) and an additional trench (the trench formed between the interlevel dielectric films 22; Fig. 4; paragraph [0026]) filled with conductive material (the conductive material of the source electrode 21; Fig. 4, paragraph [0026]), the additional trench (the trench formed between the interlevel dielectric films 22) extending through the source region (14) to the body region (13), the conductive material in the additional trench (the conductive material of the source electrode 21 in the trench) connecting the source contact (21) to the source region (14) and to the body region (13).

29. Regarding **claim 19**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) at the first major surface (the top surface of 13), a body region (well layer 13; Fig. 2, paragraph [0023]) under the source region (14), a drift region (drift layer 12; Fig. 2, paragraph [0023]) under the body region (13), and a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) under the drift region (12), the drift region (12) having a doping concentration (see Fig. 15B) that increases from a part of the drift region (12) adjacent to the body region (13) to a part of the drift region (12) adjacent to the drain region (11); and a plurality of insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) into the drift region (12), each of the insulated trenches (15) including at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) and separated from the body region (13) by a gate insulator (second insulating film

18; Fig. 2, paragraph [0024]), at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) and separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode (19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]).

Omura et al. do not teach, the doping concentration in the drift region (12) being at least 50 times greater adjacent to the drain region (11) than adjacent to the body region (13) and the gate-field plate insulator (18) being at least as thick as the field plate insulator (16).

Parameters such as the thicknesses of the gate-field plate insulator and the filed plate insulator, and the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the breakdown voltage and the threshold voltage in paragraph [0031]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thicknesses of the gate-field plate insulator and the filed plate insulator and the doping concentration within the range as claimed in order to achieve desired device performance.

30. Regarding **claim 21**, Omura et al. teach an insulated gate field effect transistor according to claim 15, wherein the drift region (12) has a steeply graded doping concentration (see Fig. 15B).

Omura et al. do not teach the drift region has a steeply graded doping concentration that is defined by the ration of the doping concentration of the part of the drift region adjacent to the

body region to the doping concentration of the part of the drift region adjacent to the drain region and wherein the ratio is greater than at least one of: 50, 100 or 200.

Parameters such as the ratio of the doping concentration of the part of the drift region adjacent to the body region to the doping concentration of the part of the drift region adjacent to the drain region in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the breakdown voltage and the threshold voltage in paragraph [0031]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the ratio of the doping concentration of the part of the drift region adjacent to the body region to the doping concentration of the part of the drift region adjacent to the drain region within the range as claimed in order to achieve desired device performance.

31. **Claims 2 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 1 above, and further in view of Onda et al. ("SIC Integrated MOSFETs" Physica Status Solidi (A), Applied Research, Berlin, DE, vol. 162, no. 1, 16 July 1997, pages 369-388).

Omura et al. teach, regarding to **claim 11**, the first conductivity type is n-type (the conductivity type of the source region; paragraph [0023]), the second conductivity type is p-type (the conductivity type of the body region; paragraph [0023]).

Omura et al. do not teach, regarding to **claim 2**, the conductive gate electrode is of conductive semiconductor doped to be the second conductivity type (i.e. p-type), and regarding to **claim 11**, the conductive gate electrode is of p-type doped polysilicon.

In the same field of endeavor of semiconductor device, Onda et al. teach the conductive gate electrode is a p-type doped polysilicon (Fig. 1, page 371 line 27). Onda et al. also teach that p-type polysilicon is used to form an accumulation mode SiC trench MOSFET (page 371, lines 23-43).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Onda et al. and use the gate taught by Onda et al., because an accumulation mode SiC trench MOSFET can be formed as taught by Onda et al.

32. **Claims 3 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claims 1and 19 above, and further in view of Miyano et al. (JP 403211885A).

Regarding **claims 3 and 20**, Omura et al. teach the conductive gate electrode and the insulated trench.

Omura et al. do not teach, regarding to **claim 3**, the conductive gate electrode has side pieces spaced apart adjacent to the sidewalls on either side of the insulated trench and a top piece spanning a gap between the side pieces, and regarding to **claim 20**, the conductive gate electrode in each of the insulated trenches includes two vertical side pieces spaced apart from each other and adjacent to sidewalls on either side of the insulated trench, and a horizontal top piece spanning a gap between and connecting the two side pieces.

In the same field of endeavor of semiconductor device, Miyano et al. teach, regarding to **claim 3**, the conductive gate electrode (gate electrode 3; Fig. 1, [Application example]) has side pieces (the left side and the right pieces with deeper depth) spaced apart adjacent to the sidewalls on either side of the insulated trench (a trench; Fig. 1 and 2, [Application example]) and a top

piece spanning a gap between the side pieces (see Fig. 1 of the middle portion of gate electrode 3 with shallower depth than the left side and the right side pieces), and regarding to **claim 20**, the conductive gate electrode (gate electrode 3; Fig. 1, [Application example]) in each of the insulated trenches (a trench; Fig. 1 and 2, [Application example]) includes two vertical side pieces (the left side and the right pieces with deeper depth) spaced apart from each other and adjacent to sidewalls on either side of the insulated trench (a trench; see Fig. 1 and 2, [Application example]), and a horizontal top piece spanning a gap between and connecting the two side pieces (see Fig. 1 of the middle portion of gate electrode 3 with shallower depth than the left side and the right side pieces).

Miyano et al. also teach the shape of the gate reduces the capacitance between the gate and the drain, i.e. the bottom structure, and a high speed operation can be performed ([Operation]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Miyano et al. and use the gate taught by Miyano et al., because the speed of the device can be improved as taught by Miyano et al.

33. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 7 above, and further in view of Hshieh et al. (US 2001/0003367 A1).

Regarding **claim 8**, Omura et al. do not teach a doped contact region of the second conductivity type in the body region in contact with the conductive material in the additional trench, a doping concentration in the doped contact region being higher than a doping concentration in the rest of the body region.

In the same field of endeavor of vertical transistors, Hshieh et al. teach a doped contact region (P+ region 138; Fig. 2, paragraph [0025]) of the second conductivity type (p type) in the body region (in the P-body region; Fig. 2, paragraph [0025]) in contact with the conductive material (source metal layer 160; Fig. 2, paragraph [0025]) in the additional trench (source contact openings 150; Fig. 2, paragraph [0025]), a doping concentration in the doped contact region being higher than a doping concentration in the rest of the body region (the doping concentration of P+ region is higher than P region). Hshieh et al. also teach the doped contact region 138 is used to reduce the parasitic resistance (paragraph [0025]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Hshieh et al. and use the doped contact region taught by Hshieh et al., because the parasitic resistance can be reduced as taught by Hshieh et al.

Response to Arguments

34. Applicant's amendments, filed 05/03/2010, overcome the objections to claims 1-18 and 20 and the rejections to claims 15-18 under 35 U.S.C. 112. The objections to claims 1-18 and 20 and the rejections to claims 15-18 under 35 U.S.C. 112 have been withdrawn. The rejections to claims 5-6 and 10 still stand because the applicant does not respond to the rejections.

35. Applicant's arguments filed 05/03/2010 have been fully considered but they are not persuasive.

36. On page 9 of Applicant's Response, Applicant argues that the '455 reference teaches away from the thickness of the gate-field plate insulator being greater than or equal to the

thickness of the field plate insulator. Firstly, the '455 reference teaches that the first insulating film 16 (i.e., the asserted field plate insulator) is preferably thicker than the second insulating film 18. Secondly, the specific example thicknesses given by the '455 reference indicate that film 16 should be substantially thicker than film 18 (e.g., 3000A versus 450A).

37. The Examiner respectfully disagrees with Applicant's argument. Firstly, the '455 reference teaches a preferred embodiment that the first insulating film 16 (i.e., the asserted field plate insulator) is thicker than the second insulating film 18, but does not teach any reason that the thickness of the gate-field plate insulator can not be greater than or equal to the thickness of the field plate insulator. It is very common for the inventor to disclose a preferred embodiment in his invention but in no way the inventor is teaching away all other embodiments not included in the preferred embodiment. In the same way, the applicant specified in the instant application a preferred embodiment of the doping concentration of the drift region is such that the doping concentration adjacent to the drift region is higher than the doping concentration adjacent to the body region by a factor of at least 100, and further preferably at least 200 (page 3, lines 15-19 of the specification of the instant application). This disclosure does not teach away a factor of at least 100 because it is less preferable and also does not teach away another embodiment of a factor of at least 50 (page 3, lines 6-10 of the specification of the instant application). Secondly, the examples are given to show the details of the embodiments and are not intended to limit the scope of the invention. An example in the reference does not teach away other examples with different values. Most importantly, '455 reference teaches that the thickness of the gate-field plate insulator 18 is determined by a threshold voltage and the thickness of the field plate insulator 16 is determined by a breakdown voltage. Thus the thicknesses of these two layers

depend on the application and for some applications (e.g. high threshold voltage and low breakdown voltage), the thickness of the gate-field plate insulator can be greater than or equal to the thickness of the filed plate insulator using the method shown by ‘455 (paragraph [0031]). Thus ‘455 does not teach away from the thickness of the gate-field plate insulator being greater than or equal to the thickness of the field plate insulator.

38. On page 10 of Applicant’s Response, Applicant argues the Office Action fails to give weight to the evidence that the '455 reference teaches away through specifically disclosing the relationship between the asserted gate field plate insulator and the asserted field plate insulator being opposite of what is claimed. Instead, the Office Action at page 18 dismisses this evidence by simply stating that the '455 reference does not forbid using a device with the field plate insulator 16 thinner than the gate-field plate insulator 18."

39. The Examiner respectfully disagrees with Applicant’s argument, because the examiner does not believe that '455 reference teaches away through specifically disclosing the relationship between the asserted gate field plate insulator and the asserted field plate insulator being opposite of what is claimed. ‘455 reference discloses preferred embodiment and examples and does not teaching away using a device with the field plate insulator 16 thinner than the gate-field plate insulator 18. ‘455 reference discloses the principle of selecting the thicknesses of gate field plate insulator and the field plate insulator and these thicknesses are determined by a specific application.

40. On page 10 of Applicant’s Response, Applicant argues that the Office Action fails to provide proper motivation for the asserted modification.

41. The Examiner respectfully disagrees with Applicant's argument, because the Examiner provided the motivation by stating that "to achieve the desired device performance' in the office action. The motivation is appropriate for routine experimentation and optimization, as this process is needed to derive the optimum range of values of parameters. The optimum range of values also depends on the specifications of the device, i.e. the desired device performance. Thus "to achieve the desired device performance' is one of the motivations for routine experimentation and optimization.

42. On page 11 of Applicant's Response, Applicant argues that the Office Action's asserted motivation and arguments indicate that the Examiner is engaging in impermissible hindsight reasoning.

43. The Examiner respectfully disagrees with Applicant's argument, because Omura et al. teach the device performances of the breakdown voltage and the threshold voltage and their relationships to the thicknesses of the gate-field plate insulator and the field plate insulator in paragraph [0031]. In order to achieve the desired device performance, e.g. specified breakdown voltage and the threshold voltage, the thicknesses of the gate-field plate insulator can be at least as thick as the thickness of the field plate insulator.

44. On page 11 of Applicant's Response, Applicant argues that the cited portions of the '455 reference do not provide any indication regarding the actual level of impurity concentration in drift layer 12 near well layer 13 relative to the actual level of impurity concentration in drift layer 12 near substrate 11, let alone teach that the doping concentration in the drift region has a steeply graded concentration gradient as in the claimed invention.

45. The Examiner respectfully disagrees with Applicant's argument, because the '455 reference teaches that the doping concentration has a graded concentration (Figs 16A to 16C) but does not teach the actual level. The reason for not specifying the steepness of the graded concentration because the actual level is commonly known by the routine experimentation and optimization which in general involves no novelty. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (MPEP 2144.05 II A).

46. On pages 11-12 of Applicant's Response, Applicant argues that Applicant's specification teaches that "[b]y providing a steeply graded concentration gradient in the drift region it is possible to achieve structures having both a low specific on-resistance and a low switching loss." Paragraph 0020 of the published application. Accordingly, Applicant's specification teaches that the gradient is critical. Therefore, the claimed concentration gradient is not obvious based on the '455 reference, and the § 103 rejections should be withdrawn.

47. The Examiner respectfully disagrees with Applicant's argument, because the criticality of the claimed range is established by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). (MPEP 2144.05 III). '455 teaches that the graded concentration can decrease the on-resistance (paragraph [0061]). The disclosure of the instant application does not show the unexpected result relative to the prior art range and the criticality of the claimed range is not established. Please see MPEP 716.02-716.02(g) for how to establish the unexpected result.

Conclusion

48. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
7/7/2010